Docket No.: 08211/0200375-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Ha Chu Vu

Patent No.: 7,271,788

Issued: September 18, 2007

For: GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.323

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted a typographical error which should be corrected. A listing of the error to be corrected is attached.

The typographical error marked with an "A" on the attached list are found in the application as filed by applicant. Payment in the amount of $100.00 covering the fee set forth in 1.20(a) is enclosed.

The error now sought to be corrected are inadvertent typographical errors the correction of which does not involve new matter or require reexamination.

Transmitted herewith is a proposed Certificate of Correction effecting such corrections. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to $300.00 or credit any excess in this fee to Deposit Account No. 04-0100.

Dated: October 17, 2007

Respectfully submitted,

By_____

Flynn Barrison
Registration No.: 53,970
DARBY & DARBY P.C.
P.O. Box 770
Church Street Station
New York, New York 10008-0770
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,271,788

APPLICATION NO.: 10/718,975

ISSUE DATE : September 18, 2007

INVENTOR(S) : Vu

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 8, line 32, in Claim 14, before "for" delete "means".

MAILING ADDRESS OF SENDER (Please do not use customer number below):
John W. Branch, Esq.
DARBY & DARBY P.C.
P.O. Box 770
Church Street Station
New York, New York 10008-0770

Darby & Darby

Issued Patent Proofing Form
Note: P = **PTO Error** A = **Applicant Error**

File#: **08211/0200375-US0**
(10/01/2007)

US Serial No.: **10/718,975** US Patent No.: **US 7,271,788 B2** Issue Dt.: **Sep. 18, 2007**
Title: **GENERATING ADJUSTABLE-DELAY CLOCK SIGNAL FOR PROCESSING COLOR SIGNALS**

Sr. No.	P/A	Original		Issued Patent		Description Of Error
		Page	Line	Column	Line	
1	A	Page 5 Claims (04/23/2007)	Claim 11 Line 1	8	32 (Approx.)	In Claim 14, before "for" delete "means".

a first switch coupled between a first node and a second node, wherein the first switch is arranged to receive the first weight signal at the first node;

a first differential pair having at least a first input, a second input, and an output, wherein the first differential pair is arranged to receive the first selected phased signal at the first input, and wherein the second input is connected to the second node;

a second switch coupled between a third node and a fourth node, wherein the second switch is arranged to receive the first weight signal at the third node;

a second differential pair having at least a first input, a second input, and an output, wherein the second differential pair is arranged to receive the first selected phased signal at the first input, and wherein the second input is connected to the fourth node;

a third switch coupled between a fifth node and a sixth node, wherein the third switch is arranged to receive the first weight signal at the fifth node; and

a third differential pair having at least a first input, a second input, and an output, wherein the third differential pair is arranged to receive the second selected phased signal at the first input, and wherein the second input is connected to the sixth node.

10. The circuit of claim **9**, wherein the phase mixer further includes:

a fourth switch coupled between a seventh node and an eighth node, wherein the fourth switch is arranged to receive the second weight signal at the seventh node; and

a fourth differential pair having at least a first input, a second input, and an output, wherein the fourth differential pair is arranged to receive the second selected phased signal at the first input, and wherein the second input is connected to the eighth node, wherein the outputs of the differential pairs are connected to an output bus.

11. The circuit in claim **9**, wherein the at least one selected phase information signal activates one of the first differential pair or the second differential pair, wherein if the first differential pair is activated, the first switch is closed and the second switch is open, and wherein if the second differential pair is activated, the first switch is open and the second switch is closed.

12. The circuit of claim **1**, further comprising:

an analog to digital converter adapted to improve processing of the input signal by choosing an adjustment to the delay signal.

13. An interface circuit for processing an analog color signal, comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the analog color signal;

a phase adjuster adapted to generate an adjustable delay signal from two of the plurality of phased signals that are apart from each other by an odd multiple of approximately 45 degrees, wherein the phase adjuster includes:

a first phase selector for selecting a first one of the phased signals;

a second phase selector for selecting a second one of the phased signals; and

a phase mixer for multiplying the first selected phased signal with a first weight, multiplying the second selected phased signal with a second weight, and adding together the first and the second multiplied phased signals to derive the adjustable delay signal; wherein the first selected phased signal, the second selected phased signal, and at least one selected phase information signal are received into the phase mixer; and

a decoder to generate phase selection signals for selecting the first and second phased signals; and

an analog to digital converter adapted to improve processing of the analog color signal by choosing an adjustment to the delay signal, wherein at least one simulated phase signal is provided.

14. A device comprising:

means for deriving a plurality of phased signals from a synchronizing signal associated with an input signal, wherein the PLL is arranged to provide each phased signal of the plurality of phased signals on at least one corresponding separate signal line of a plurality of signal lines;

means for deriving an adjustable delay signal including:

means for selecting a first one of the phased signals;

means for selecting a second one of the phased signals; and

mixing means including:

means for multiplying the first selected phased signal with a first weight;

means for multiplying the second selected phased signal with a second weight; and

means for adding together the first and the second multiplied phased signals to derive the adjustable delay signal, wherein the first selected phased signal, the second selected phased signal, and at least one selected phase information signal are received into the mixing means

means for choosing an adjustment to the adjustable delay signal, wherein at least one simulated phase signal is provided.

15. The device of claim **14**, wherein

the means for deriving the phased signals includes phase locked loop (PLL) circuit.

16. A method for generating a delay signal for processing an input signal, comprising:

deriving a plurality of phased signals from a synchronizing signal associated with the input signal, wherein the PLL is arranged to provide each phased signal of the plurality of phased signals on at least one corresponding separate signal line of a plurality of signal lines;

deriving the delay signal from two of the plurality of phased signals including:

selecting two phased signals from the plurality of phased signals;

providing at least one selected phase information signal;

multiplying a first one of the selected phased signals with a first weight, wherein the first weight is based, at least in part, on the at least one selected phase information signal;

multiplying a second one of the selected phased signals with a second weight, wherein the second weight is based, at least in part, on the at least one selected phase information signal; and

adding together the first and the second multiplied phased signals; and

choosing an adjustment to the delay signal to improve conversion of the input signal into digital form, wherein at least one simulated phase signal is provided.

17. The method of claim **16**, wherein

the phased signals are derived in a phase locked loop (PLL) circuit.